

CLAIMS

1. A method of generating a deep N-well pattern for an integrated circuit design, said method comprising:

specifying a tile comprising a first layer wherein said first layer comprises a first layer element for a deep N-well pattern;

arranging multiple instances of said tile to create a tile array covering a portion of said integrated circuit design; and

merging said tiles to produce a deep N-well pattern.

2. The method of Claim 1, wherein said tile further comprises a second layer, wherein said second layer comprises a second layer element.

3. The method of Claim 2, wherein said first layer element is identical in shape to said second layer element.

4. The method of Claim 3, wherein said first layer element is disposed rotated with respect to said second layer element.

5. The method of Claim 1, further comprising editing said tile array.

6. The method of Claim 2, further comprising editing said first layer.

7. The method of Claim 2, further comprising editing said second layer.

8. The method of Claim 2, further comprising flattening said first layer and said second layer.

9. The method of Claim 1, wherein said specifying, arranging, and merging are performed using a computer aided design tool.

10. The method of Claim 1, further comprising performing a design rule check by incrementally expanding an opening in said deep N-well pattern.

11. A computer-readable medium comprising computer-executable instructions stored therein for performing a

method of generating a deep N-well pattern for an integrated circuit design, said method comprising:

accepting dimensional input for a tile from a user;
specifying a tile using said dimensional input, said tile comprising a first layer, wherein said first layer comprises a first layer element for a deep N-well pattern;

arranging multiple instances of said tile to create a tile array covering a portion of said integrated circuit design; and

merging said tiles to produce a deep N-well pattern.

12. The medium of Claim 11, wherein said tile comprises a second layer, wherein said second layer comprises a second layer element.

13. The medium of Claim 12, wherein said first layer element is identical in shape to said second layer element.

14. The medium of Claim 13, wherein said first layer element is rotated with respect to said second layer element.

15. The medium of Claim 11, further comprising editing said tile array.

16. The medium of Claim 12, further comprising editing said first layer.

17. The medium of Claim 12, further comprising editing said second layer.

18. The medium of Claim 12, further comprising flattening said first layer and said second layer.

19. The medium of Claim 11, wherein said specifying, arranging, and merging are performed using a computer aided design tool.

20. A method of generating a deep N-well pattern for an integrated circuit design, said method comprising:

specifying a tile;

creating tile array using the specified tile;

editing said tile array;

merging said tile array to produce a plurality of layers;

performing design rule checks on said layers;

editing said layers; and

flattening said layers to produce a finished pattern.

21. The method of Claim 20, wherein said editing comprises removing tiles that are not connected to surface N-wells.

22. The method of Claim 20, wherein said editing comprises removing tiles to provide isolation for analog devices.

23. The method of Claim 20, wherein said editing is done to isolate surface N-wells from body-bias.

24. The method of Claim 20, wherein said performing design rule checks comprises incrementally adjusting the size or position of an extended shape on one or more layers.